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- 1 [Curriculum 68: Recommendations for academic programs in computer science: a report of the ACM curriculum committee on computer science](#)   
William F. Atchison, Samuel D. Conte, John W. Hamblen, Thomas E. Hull, Thomas A. Keenan, William B. Kehl, Edward J. McCluskey, Silvio O. Navarro, Werner C. Rheinboldt, Earl J. Schweppe, William Viavant, David M. Young  
March 1968 **Communications of the ACM**, Volume 11 Issue 3  
Full text available:  [pdf\(6.63 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#)


**Keywords:** computer science academic programs, computer science bibliographies, computer science courses, computer science curriculum, computer science education, computer science graduate programs, computer science undergraduate programs

- 2 [Decision Trees and Diagrams](#)   
Bernard M. E. Moret  
December 1982 **ACM Computing Surveys (CSUR)**, Volume 14 Issue 4  
Full text available:  [pdf\(2.68 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)


- 3 [Formal verification in hardware design: a survey](#)   
Christoph Kern, Mark R. Greenstreet  
April 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 2  
Full text available:  [pdf\(411.53 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In recent years, formal methods have emerged as an alternative approach to ensuring the quality and correctness of hardware designs, overcoming some of the limitations of traditional validation techniques such as simulation and testing. There are two main aspects to the application of formal methods in a design process: the formal framework used to specify desired properties of a design and the verification techniques and tools used to reason about the relationship between a spec ...

**Keywords:** case studies, formal methods, formal verification, hardware verification, language containment, model checking, survey, theorem proving

- 4 [Data and memory optimization techniques for embedded systems](#) 

P. R. Panda, F. Catthoor, N. D. Dutt, K. Danckaert, E. Brockmeyer, C. Kulkarni, A. Vandercappelle, P. G. Kjeldsberg  
April 2001 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 6 Issue 2

Full text available:  [pdf\(339.91 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)


We present a survey of the state-of-the-art techniques used in performing data and memory-related optimizations in embedded systems. The optimizations are targeted directly or indirectly at the memory subsystem, and impact one or more out of three important cost metrics: area, performance, and power dissipation of the resulting implementation. We first examine architecture-independent optimizations in the form of code transformations. We next cover a broad spectrum of optimizati ...

**Keywords:** DRAM, SRAM, address generation, allocation, architecture exploration, code transformation, data cache, data optimization, high-level synthesis, memory architecture customization, memory power dissipation, register file, size estimation, survey

## 5 System architectures for computer music

John W. Gordon

June 1985 **ACM Computing Surveys (CSUR)**, Volume 17 Issue 2


Full text available:  [pdf\(4.61 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

Computer music is a relatively new field. While a large proportion of the public is aware of computer music in one form or another, there seems to be a need for a better understanding of its capabilities and limitations in terms of synthesis, performance, and recording hardware. This article addresses that need by surveying and discussing the architecture of existing computer music systems. System requirements vary according to what the system will be used for. Common uses for co ...

## 6 IS '97: model curriculum and guidelines for undergraduate degree programs in information systems

Gordon B. Davis, John T. Gorgone, J. Daniel Couger, David L. Feinstein, Herbert E. Longenecker

December 1996 **ACM SIGMIS Database , Guidelines for undergraduate degree programs on Model curriculum and guidelines for undergraduate degree programs in information systems**, Volume 28 Issue 1

Full text available:  [pdf\(7.24 MB\)](#) Additional Information: [full citation](#), [citations](#)

## 7 MPEG-4: an object-based multimedia coding standard supporting mobile applications

Atul Puri, Alexandros Eleftheriadis

June 1998 **Mobile Networks and Applications**, Volume 3 Issue 1

Full text available:  [pdf\(747.80 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#), [review](#)

The ISO MPEG committee, after successful completion of the MPEG-1 and the MPEG-2 standards is currently working on MPEG-4, the third MPEG standard. Originally, MPEG-4 was conceived to be a standard for coding of limited complexity audio-visual scenes at very low bit-rates; however, in July 1994, its scope was expanded to include coding of scenes as a collection of individual audio-visual objects and enabling a range of advanced functionalities not supported by other standards. One of the ke ...

## 8 Software reuse

Charles W. Krueger

June 1992 **ACM Computing Surveys (CSUR)**, Volume 24 Issue 2

Full text available:  [pdf\(4.96 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index](#)

terms


Software reuse is the process of creating software systems from existing software rather than building software systems from scratch. This simple yet powerful vision was introduced in 1968. Software reuse has, however, failed to become a standard software engineering practice. In an attempt to understand why, researchers have renewed their interest in software reuse and in the obstacles to implementing it. This paper surveys the different approaches to software reuse found in the ...

**Keywords:** abstraction, cognitive distance, software reuse

9 Computer Communication Networks: Approaches, Objectives, and Performance Considerations

Stephen R. Kimbleton, G. Michael Schneider

September 1975 **ACM Computing Surveys (CSUR)**, Volume 7 Issue 3

Full text available:  pdf(3.99 MB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)



10 A general approach for regularity extraction in datapath circuits

Amit Chowdhary, Sudhakar Kale, Phani Saripella, Naresh Sehgal, Rajesh Gupta

November 1998 **Proceedings of the 1998 IEEE/ACM international conference on Computer-aided design**

Full text available:  pdf(983.12 KB)

Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)



11 Bounds on delays and queue lengths in input-queued cell switches

Emilio Leonardi, Marco Mellia, Fabio Neri, Marco Ajmone Marsan

July 2003 **Journal of the ACM (JACM)**, Volume 50 Issue 4

Full text available:  pdf(338.26 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

In this article, we develop a general methodology, mainly based upon Lyapunov functions, to derive bounds on average delays, and on averages and variances of queue lengths in complex systems of queues. We apply this methodology to cell-based switches and routers, considering first output-queued (OQ) architectures, in order to provide a simple example of our methodology, and then both input-queued (IQ), and combined input/output queued (CIOQ) architectures. These latter switching architectures re ...

**Keywords:** Performance evaluation, delay bounds, input queued switches, scheduling



12 Robotics: a closer look at microprocessor systems

Carl W. Steidley

March 1991 **ACM SIGCSE Bulletin , Proceedings of the twenty-second SIGCSE technical symposium on Computer science education**, Volume 23 Issue 1

Full text available:  pdf(662.27 KB)


Additional Information: [full citation](#), [references](#), [index terms](#)



13 Tree-based mapping of algorithms to predefined structures

Peter Marwedel

November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**

Full text available:  pdf(693.29 KB)

Additional Information: [full citation](#), [references](#), [citations](#)



14 Instruction set extraction from programmable structures



Peter Marwedel, Rainer Leupers


September 1994 **Proceedings of the conference on European design automation**

Full text available:  [pdf\(687.28 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

15 From VHDL to efficient and first-time-right designs: a formal approach

Peter F. A. Middelhoek, Sreeranga P. Rajan

April 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 2

Full text available:  [pdf\(722.99 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

In this article we provide a practical transformational approach to the synthesis of correct synchronous digital hardware designs from high-level specifications. We do this while taking into account the complete life cycle of a design from early prototype to full custom implementation. Besides time-to-market, both flexibility with respect to target architecture and efficiency issues are addressed by the methodology. The utilization of user-selected behavior-preserving transformation steps e ...

**Keywords:** CDFG, SFG, VHDL, correctness by construction, design methodology, rapid system prototyping, transformational design

16 All-optical networks

Samir Chatterjee, Suzanne Pawlowski

June 1999 **Communications of the ACM**, Volume 42 Issue 6

Full text available:  [pdf\(296.73 KB\)](#)  [html\(42.58 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#), [review](#)

17 Optical computational geometry

Y. B. Karasik, M. Sharir

July 1992 **Proceedings of the eighth annual symposium on Computational geometry**

Full text available:  [pdf\(934.20 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

18 The UCLA Brain Research Institute data processing laboratory

T. Estrin

December 1987 **Proceedings of ACM conference on History of medical informatics**

Full text available:  [pdf\(1.09 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The Brain Research Institute is an interdisciplinary research unit of the UCLA Medical School, supporting basic research in fields which contribute to an understanding of brain mechanisms and behavior. In 1960 the School of Medicine was relatively young, having graduated its first class in 1955. Among the early professors to affiliate with the new medical school was Dr. H. W. Magoun, whose own research interests were in the nervous system. Under his leadership, a formal proposal was prepare ...

19 Dynamically reconfigurable architecture for image processor applications

Alexandro M. S. Adário, Eduardo L. Roehe, Sergio Bampi

June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available:  [pdf\(645.23 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

**Keywords:** FPGA, image processing, reconfigurable architecture

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*Tsotras, V.J.; Gopinath, B.; Hart, G.W.;*

Parallel and Distributed Processing, 1990. Proceedings of the Second IEEE Symposium on , 9-13 Dec. 1990

Pages:634 - 641

[\[Abstract\]](#)   [\[PDF Full-Text \(488 KB\)\]](#)   IEEE CNF

### 2 A new parallel computation model on synchronous wireless interconnection

*Lih-Chyau Wu; Shing-Tsaan Huang;*

TENCON '93. Proceedings. Computer, Communication, Control and Power Engineering. 1993 IEEE Region 10 Conference on , Issue: 0 , 19-21 Oct. 1993

Pages:158 - 161 vol.3

[\[Abstract\]](#)   [\[PDF Full-Text \(320 KB\)\]](#)   IEEE CNF

### 3 A note on the application of the Hilbert transform to time delay estimation

*Cabot, R.;*

Acoustics, Speech, and Signal Processing [see also IEEE Transactions on Signal Processing], IEEE Transactions on , Volume: 29 , Issue: 3 , Jun 1981

Pages:607 - 609

[\[Abstract\]](#)   [\[PDF Full-Text \(384 KB\)\]](#)   IEEE JNL

### 4 Efficient parallel pipelinable VLSI architecture for finding the maximum binary number

*Daneshgaran, F.; Yao, K.;*

Circuits, Devices and Systems, IEE Proceedings [see also IEE Proceedings G-Circuits, Devices and Systems] , Volume: 141 , Issue: 6 , Dec. 1994

Pages:527 - 534

[\[Abstract\]](#)   [\[PDF Full-Text \(564 KB\)\]](#)   **IEEE JNL**

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